

LIQUID CRYSTAL DISPLAY DEVICE

BACKGROUND OF THE INVENTION

The present invention relates to a liquid crystal display device capable of reducing a consumption power.

As shown in Fig.2, a liquid crystal display (LCD) controller 203 is connected with an LCD unit 205, an image data memory 202, a micro-processing unit (MPU) 201 and a synchronizing signal generator circuit 204. Under commands of MPU 201, image data stored in the image data memory 202 is input to the LCD controller 203 and is signal-converted, so that the converted image data is displayed on the LCD unit 205.

In a conventional LCD controller, when the same (frame) image data is displayed on the LCD unit for a long time, (1) the display is continued, or (2) after an input interruption from a keyboard a mouse or the like is monitored and a desired period of time elapses, driving of a liquid crystal is stopped after the displayed image data is restored in the memory, or a backlight unit is turned off.

In the same frame image display for a long time, a method other than an image data restorage to the memory and a turning off of a backlight unit does not provide power saving of an LCD unit. Therefore, a frame image storage method for providing power saving without using unnecessary memories is desired. Also, since a backlight unit is not always included in all LCD devices, a method for providing power saving in a case wherein the same frame image is displayed for a long time, other than turning off of the backlight unit, is desired.

SUMMARY OF THE INVENTION

The object of the present invention is to solve the above problem.

According to the present invention, a liquid crystal display device of Fig.1 includes, a micro-processing unit (MPU) 101 for controlling a whole peripheral circuit, an image data memory 102 capable of storing two frame image data, an image data arranging circuit 103 for arranging two frame image data, an image data

comparator circuit 104 capable of comparing two frame image data in bit units, a timer circuit 106, a liquid crystal display (LCD) unit 110, an LCD controller 107 for controlling the LCD unit 110, a synchronizing signal generator circuit 109 for generating synchronizing signals (vertical and horizontal synchronizing signals), and a synchronizing signal regulating circuit 108 for regulating vertical and horizontal synchronizing signals in accordance with an output signal from the circuit 104. An output signal from the circuit 108 is input to the LCD controller 107, to control synchronizing signals to the LCD unit 110.

In the above structure, a peripheral circuit in an LCD device represents a circuit having a function for driving a display portion constructing the LCD unit. The display portion in the LCD device has a structure which pixels constructed by a liquid crystal arranged between at least one pair of electrodes are arranged at a matrix form. As a structure of the display portion, there is two types. One is a simple matrix type, and the other is an active matrix type.

Basically, an LCD unit includes analog buffers for driving each liquid crystal pixel arranged at a matrix form, analog memories for storing images to be displayed, and shift registers for generating operation timings of a matrix circuit in an X and Y directions. Also, a peripheral circuit in the LCD device includes an LCD controller for supplying data and clocks for the shift registers of X and Y directions to the LCD unit, a synchronizing signal generating circuit for supplying horizontal and vertical synchronizing signals and timing signals to the LCD controller, and an image data memory for storing images to be displayed.

The above structure can be used in a simple matrix type or an active matrix type LCD device. A liquid crystal material to be used is not limited to a specific material.

A memory element capable of storing two frame image data has a function for storing two frame image data necessary to display

two frames. As the memory element, a video random access memory (VRAM) is used. The VRAM is of a dynamic random access memory (DRAM) and has normal parallel input and output ports, and further serial input and output ports.

Two frame image data stored in the image data memory 102 are compared with each other in bit units by the image data comparator circuit 104, and then the circuit 104 outputs an output signal representing a comparison result. In accordance with the output signal, the synchronizing signal regulator circuit 108 regulates horizontal and vertical synchronizing signals and supplies the regulated horizontal and vertical synchronizing signals to the LCD controller 107.

In a case wherein the same frame is displayed for a long time, if the number of scannings on a display portion (screen) of the LCD device is decreased, a consumption power can be reduced.

A time to decrease the number of scannings is set by the timer circuit 106, a time interval that characteristics of a liquid crystal does not deteriorate without applying an alternating voltage to a liquid crystal in an LCD device, a refreshing time of a memory for storing image data in a peripheral circuit of the LCD device, or a refreshing time of an analog memory included in the LCD unit can be selected and set.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig.1 shows a block diagram of a liquid crystal display (LCD) device according to an embodiment of the present invention;

Fig.2 shows a block diagram of a convention LCD device;

Fig.3 shows a block diagram of an LCD device according to another embodiment;

Fig.4 shows a block diagram of an image data arranging circuit in the LCD device of Fig.3;

Fig.5 shows a block diagram of an image data comparator circuit in the LCD device of Fig.3; and

Fig.6 shows a block diagram of an LCD device according to

another embodiment.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[Embodiment 1]

In a peripheral circuit for a liquid crystal display (LCD) device as shown in Fig.3, a video random access memory (VRAM) 301 is used as an image data memory element, an image data arranging circuit is constructed by a first in first out (FIFO) circuit 302, an image data comparator circuit is constructed by a comparator circuit 304, and a synchronizing signal regulator circuit is constructed by AND circuits 305. Further, the LCD device includes an LCD controller 306, an LCD unit 307 having a backlight unit 307a, a timer 308 including a counter (not shown), and a synchronizing signal generator circuit 309.

An operation of the device of Fig.3 is described below.

The LCD controller 306 performs image data read to the VRAM 301. Image data read out from the VRAM 301 is input to the FIFO circuit 302.

Fig.4 shows a structure of the FIFO circuit 302. The FIFO circuit 302 is constructed by an FIFO selector 401, FIFO0 402 and FIFO1 403, and flipflop (FF) circuits 404 and 405. The FIFO selector 401 switches to store the first frame into the FIFO0 402 and store the second (next) frame into the FIFO1 403. When data is input to the FIFO1 403, the FIFO0 402 and the FIFO1 403 are set to obtain an enable state with respect to data output. Data from the FIFO0 402 and the FIFO1 403 are synchronized and output from the flipflop circuits 404 and 405 in accordance with a standard clock.

Output data signal from the FIFO circuit 302 is input to the comparator circuit 304 as shown in Fig.5. The comparator circuit 304 includes two comparators 501a and 501b, two AND (gate) circuits 502a and 502b, two flipflop (FF) circuits 503a and 503b, and delay circuits 504a and 504b for delaying a comparator circuit output. Each two circuits are used to regulate horizontal and vertical synchronizing signals. The delay circuit 504a and 504b are used to output signals in

synchronous with a standard clock, to prevent an element delay or the like in a case wherein a comparison result of two frame images is output accurately.

Image data signals in bit units with respect to two frame images are compared with each other by the comparators 501a and 501b. The AND circuits 502a and 502b output a low level (L) signal when the two image data signals coincide with each other, and output a high level (H) signal when the two image data signals are different from each other. The two output signals are synchronized with a standard clock by the flipflop circuits 503a and 503b and are output through the delay circuits 504a and 504b. Therefore, in the comparator circuit 304, two frame images are compared with each other and a level representing whether or not the two frame images coincide with each other can be determined.

Output signals from the comparator circuit 304 are input to a synchronizing signal regulator circuit 305 constructed by the AND circuits. As shown in Fig.3, in the AND circuits 305, an AND logic operation is performed between the output signals from the circuit 304 and the horizontal and vertical synchronizing signals from the synchronizing signal generator circuit 309.

As described above, when two image data signals coincide with each other, a low level (L) signal is output from the comparator circuit 304. Therefore, when an AND logic operation is performed in the AND circuits 305, the horizontal and vertical synchronizing signals are not output from the AND circuits 305 to the LCD controller 306. Only vertical synchronizing signal may be not output.

On the other hand, when the two image data signals are different from each other, a high level (H) signal is output from the comparator circuit 304. Therefore, when an AND logic operation is performed in the AND circuits 305, the horizontal and vertical synchronizing signals are output from the AND circuits 305 to the LCD controller 306.

In either of the above states, the horizontal and vertical

synchronizing signals are input to the LCD unit 307 through the LCD controller 306.

When two image data coincide with each other, the timer 308 starts count and horizontal and vertical synchronizing signals are maintained at the same state until a count value of the timer 308 reaches a set value. The timer 308 is connected with the comparator circuit 304 through an interruption signal line 320. When the count value of the timer 308 reaches the set value, an interruption signal output from the timer 308 changes an output signal level of the comparator circuit 304 into a high level (H).

Also, when two image data coincide with each other, since the timer 308 is connected with the LCD unit 307 through a backlight unit switch line 321, the timer 308 outputs a signal (having a level for turning off a backlight unit 307a) to the backlight unit switch line 321 after a count value of the timer 308 reaches an initial set value, so that the backlight unit 307a of the LCD unit 307 can be turned off. When the timer 308 is reset, the level of the signal on the backlight unit switch line 321 is held to a level for turning on the backlight unit 307a.

By the above operations, when the same frame images are continuous, turning on and off of the backlight unit 307a can be controlled.

[Embodiment 2]

In Fig.6, VRAMs 602 and 603 are arranged as an image data memory element, and the first frame image and the second (next) frame image are stored in the VRAMs 602 and 603, respectively, by a VRAM input selector 601 for selecting the VRAM 602 and 603. Since the VRAMs 602 and 603 are used in an LCD device of Fig.6, the image data arranging circuit of Fig.1 is not necessary. The image data comparator circuit is constructed by a comparator circuit 606, and the synchronizing signal regulator circuit is constructed by AND (gate) circuits 607. Further, the LCD device includes a VRAM output selector 604, an LCD controller 608, an

LCD unit 609 having a backlight unit 609a, a timer circuit 610 and a synchronizing signal generator circuit 611.

An operation of the LCD device of Fig.6 is described.

Continuous image data are input to the VRAM input selector 601 from a MPU bus connected with a MPU (not shown). An even frame image is stored in the VRAM 602, and an odd frame image is stored in the VRAM 603.

The image data stored in the VRAMs 602 and 603 are input to the comparator circuit 606 and the VRAM output selector 604. The VRAM output selector 604 is a circuit for alternately reading out the image data from VRAMs 602 and 603 in response to a data readout signal from the LCD controller 608.

The comparator circuit 606 is the same structure as the comparator circuit 304 and is shown in Fig.5. Two frame image data (in bit units) read out from the VRAMs 602 and 603 are compared with each other by the comparators 501a and 502b. In the comparators 501a and 501b, when two image data signals coincide with each other, a low level (L) signal is output, and when the two image data signals are different from each other, a high level (H) signal is output. Two output signals are synchronized with a standard clock by the flipflop circuits 503a and 503b and output through the delay circuits 504a and 504b for comparator circuit delay.

By the above operation, a level whether or not two frame images coincide with each other can be determined.

Output signals from the comparator circuit 606 are input to the synchronizing signal regulator circuit 607. As shown in Fig.6, an AND logic operation between the output signal from the circuit 606 and horizontal and vertical synchronizing signals from the synchronizing signal generator circuit 611 is performed in the AND circuits 607.

As described above, when two image data signals coincide with each other, a low level (L) signal is output from the comparator circuit 606. Therefore, when an AND logic operation is performed in the AND circuits 607, the horizontal and

vertical synchronizing signals are not output from the AND circuits 607 to the LCD controller 608. Only vertical synchronizing signal may be not output.

On the other hand, when the two image data signals are different from each other, a high level (H) signal is output from the comparator circuit 606. Therefore, when an AND logic operation is performed in the AND circuits 607, the horizontal and vertical synchronizing signals are output from the AND circuits 607 to the LCD controller 608.

In either of the above states, the horizontal and vertical synchronizing signals are input to the LCD unit 609 through the LCD controller 608.

When two image data coincide with each other, the timer circuit 610 starts count and horizontal and vertical synchronizing signals are maintained at the same state until a count value of the timer circuit 610 reaches a set value. The timer circuit 610 is connected with the comparator circuit 606 through an interruption signal line 620. When the count value of the timer circuit 610 reaches the set value, an interruption signal output from the timer circuit 610 changes an output signal level of the comparator circuit 606 into a high level (H).

Also, when the two image data coincide with each other, since the timer circuit 610 is connected with the LCD unit 609 through a backlight unit switch line 621, the timer circuit 610 outputs a signal (having a level for turning off the backlight unit 609a) to the backlight unit switch line 621 after a count value of the timer circuit 610 reaches an initial set value, so that the backlight unit 609a of the LCD unit 609 can be turned off. When the timer circuit 610 is reset, the level of the signal on the backlight unit switch line 621 is held to a level for turning on the backlight unit 609a.

By the above operations, when the same frame images are continuous, turning on and off of the backlight unit 609a can be controlled.

